CLAIMS

1-44. (Cancelled)

45. (Previously Presented) A semiconductor device comprising:

an insulating layer;

an ammonia-cleaned, etched opening in said insulating layer; and

a conductor in said ammonia-cleaned, etched opening.

46. (Previously Presented) An integrated circuit comprising:

an ammonia-cleaned, etch residue-free High Aspect Ratio opening provided in an insulating layer, said opening being formed over a polysilicon region; and

a conductor within said opening, said conductor being electrically connected with said polysilicon region.

47. (Previously Presented) An integrated circuit as in claim 46 further comprising a silicide layer between said conductor and said polysilicon region.

48. (Original) An integrated circuit as in claim 46, wherein said integrated circuit is a memory circuit.

49. (Original) An integrated circuit as in claim 47 wherein the interface area between said conductor and polysilicon region is free of oxygen contamination.

50-53. (Cancelled)

AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to Figures 9A-10C.

Attachment: Replacement sheets

Annotated sheets with red-ink are provided. Note, changes are only to drawing quality. The attached replacement drawings were accepted in the parent application, as indicated by the attached USPTO paper.